## **CLAIMS**

## What is claimed is:

1. A processor, comprising:

fetch logic that retrieves instructions from memory;

decode logic coupled to said fetch logic; and

an active program counter selected as either a first program counter or a second program counter;

wherein an instruction is replaced by a micro-sequence comprising one or more instructions and the active program counter switches between the first and second program counters.

- 2. The processor of claim 1 further including a vector table accessible by said decode logic, said vector table including information which specifies whether an instruction is to be replaced by a micro-sequence.
- 3. The processor of claim 2 wherein the information is provided to the vector table from a block of memory accessible to the processor by an indirect addressing mode used in a repeat loop comprising at least one instruction.
- 4. The processor of claim 2 wherein the vector table comprises a plurality of entries and any one entry can be modified independently of the other entries.

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- 5. The processor of claim 1 further including a micro-sequence vector table comprising a plurality of entries, each entry corresponding to a separate instruction and associated with a bit indicating whether the corresponding instruction is to be executed by the processor or whether the instruction is to be replaced by a micro-sequence.
- The processor of claim 5 wherein at least some of the entries include a reference to a memory location in which a micro-sequence is stored depending if the associated bit indicates that the instruction is to be replaced by a micro-sequence.
- 7. The processor of claim 1 wherein the active program counter again switches between the first and second program counters when the micro-sequence is completed.
- 8. The processor of claim 1 wherein the second program counter is used to fetch and decode instructions comprising a micro-sequence and switching between the first and second program counters comprises switching from the first program counter to the second program counter and loading the second program counter with a starting address of the micro-sequence.
- 9. The processor of claim 1 wherein a plurality of instructions are replaceable by a corresponding micro-sequence.
- 10. A method, comprising:fetching an instruction; and

determining whether said instruction is to be executed or replaced by a group of other instructions.

- 11. The method of claim 10 further including replacing the instruction with said group of other instructions.
- 12. The method of claim 10 wherein determining whether the instruction is to be executed or replaced includes determining a value of a bit associated with the instruction.
- 13. The method of claim 10 further including switching an active program counter between two program counters when replacing the instruction with the group of instructions.
- 14. The method of claim 10 further including programming a table to specify which instructions are to be executed directly and which instructions are to be replaced a group of instructions.
- 15. A system, comprising:
  - a first processor; and
  - a second processor coupled to said first processor, said second processor comprising:

fetch logic that retrieves instructions from memory;

decode logic coupled to said fetch logic; and

an active program counter selected as either a first program counter or a second program counter;

wherein an instruction is replaced by a micro-sequence comprising one or more instructions and the active program counter switches between the first and second program counters.

- 16. The system of claim 15 wherein said second processor further includes a micro-sequence vector table comprising a plurality of entries, each entry corresponding to a separate instruction and including a field that indicates whether the corresponding instruction is to be executed by the second processor or whether the instruction is to be replaced by a micro-sequence.
- 17. The system of claim 16 wherein each entry also includes a reference to a memory location in which a micro-sequence is stored depending on a value stored in the field.
- 18. An electronic device, comprising:

decode logic that decodes instructions; and

- a vector table comprising a plurality of entries, each entry corresponding to a separate instruction and including a first field indicating whether the corresponding instruction is to be executed by the electronic device or whether the instruction is to be replaced by a predetermined group of instructions stored in memory.
- 19. The electronic device of claim 18 further including an active program counter selected as either a first program counter or a second program counter, wherein an instruction is replaced by the group of instructions and the active program counter concurrently switches from the first to the second program counter.

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- 20. The electronic device of claim 18 wherein upon switching the active program counter, the first program counter is incremented.
- 21. The electronic device of claim 18 wherein the group of instructions terminates with a predetermined instruction.
- 22. A processor, comprising:

decode logic that decodes instructions; and

- a means for determining whether an instruction is to be executed or replaced by a microsequence of other instructions.
- 23. The processor of claim 22 further including a means for replacing the instruction with the micro-sequence.

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